Register Map for the CIO-DAS08/JR and CIO-DAS08/JR-AO

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Register Description

All of the programmable functions of the CIO-DAS08/JR and CIO-DAS08/JR-AO are accessible through the control and data registers.

Register level programming should be attempted only by experienced programmers. As an alternative to register level programming, the CIO-DAS08/JR and CIO-DAS08/JR-AO board are fully supported by the Universal Library software as well as most high-level data acquisition and control application packages.

Register Layout

The CIO-DAS08/JR is controlled and monitored by writing to and reading from four consecutive 8-bit I/O addresses, and the CIO-DAS08/JR-AO is controlled and monitored by writing to and reading from eight consecutive 8-bit I/O addresses. The first address, or *Base Address*, is determined by setting a bank of switches on the board.

Most often, register manipulation is best left to *Assembly* language programs, as most possible functions are implemented in Universal Library routines.

Note that an "X" is an unspecified bit. There is no function associated with that bit position. All X bits should be masked out of reads.

To write to or read from a register in decimal or HEX, the following weights apply:

Table 1. Bit weights

Bit Position	Decimal Value	Hex Value
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write control words or data to a register, the individual bits must be set to 0 or 1, and then combined to form a byte. Data read from registers must be analyzed to determine which bits are on or off.

The registers and their function are listed in Table 2. Each register has eight bits which may constitute a byte of data or eight individual bit set/read functions.

Table 2. Board registers

Address	Read Function	Write Function
Base	A/D Bits 8-11 (LSB)	None
Base + 1	A/D Bits 0 (MSB) - 7	Start 12 bit A/D conversion
Base + 2	A/D status & MUX Address	Set A/D channel
Base + 3	Digital input, 8 bits	Digital output, 8 bits
Base + 4		D/A 0 LSB (-AO only)
Base + 5		D/A 0 MSB (-AO only)
Base + 6		D/A 1 LSB (-AO only)
Base + 7		D/A 1 MSB (-AO only)

A/D Registers

Base Address

7	6	5	4	3	2	1	0
A/D8	A/D9	A/D10	A/D11 LSB	X	X	X	X

A read only register.

On a read, it supplies the least significant four digits of the analog input data. These four bits of analog input data must be combined with the eight bits of analog input data in Base + 1 to form a complete 12-bit number. The data is in the format 0 = minus FS (full scale); 4095 = +FS.

Base Address + 1

7	6	5	4	3	2	1	0
A/D0 MSB	A/D1	A/D2	A/D3	A/D4	A/D5	A/D6	A/D7

Read: The most significant A/D byte is read.

Write: Any write to this register causes an immediate A/D conversion.

Caution: Place several NO-OP instructions between consecutive 12-bit A/D conversions to avoid over-running the A/D converter.

Status and Control Register

Base Address + 2

This register address is two registers — one for reading and one for writing.

Read = Status

7	6	5	4	3	2	1	0
EOC	X	X	X	X	ChAdd2	ChAdd1	ChAdd0

EOC = 1 The A/D is busy converting and data should not be read.

EOC = 0 The A/D is not busy and data may be read.

ChAdd 2 to ChAdd 0 The current analog input multiplexer channel. The current channel is a binary coded number between 0 and 7.

Write = Control

7	6	5	4	3	2	1	0
X	X	X	X	X	ChAdd2	ChAdd1	ChAdd0

ChAdd 2 to ChAdd 0 Set the current channel address by writing a binary coded number between 0 and 7 to these three bits.

Digital I/O Control Register

Base Address + 3

This address contains two registers, one for output and one for input. The output register is latched and holds the last value written to it. The input register is not latched. Each time the register is read the current state of the inputs is passed through this port into the computer.

Write = Set digital output port, all bits.

Read = Read digital input port, all bits, and update both D/A channels simultaneously with the last values written to the D/A output registers.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

D/A Control Registers (CIO-DAS08/JR-AO only)

Each D/A is controlled by a pair of 8-bit write only registers. These registers contain the high nibble and the low byte of the D/A 12 bit control word. The value written to these two registers controls the output of the D/A chip.

To update the D/A outputs with the values in the D/A output registers, read the register at Base + 3.

The D/A output range can be calculated as [(#/4096) * 10V] – 5V (for # between 0 and 4095 inclusive). The #/4096 is a proportion of the Full Scale Range, which is ±5V.

D/A 0 Control Registers

Base Address + 4, DAC 0 Low Byte

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0 LSB

Base Address + 5, DAC 0 High Byte

7	6	5	4	3	2	1	0
X	X	X	X	DA11 MSB	DA10	DA9	DA8

D/A 1 Control Registers

Base Address + 6, DAC 1 Low Byte

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0 LSB

Base Address + 7, DAC 1 High Byte

7	6	5	4	3	2	1	0
X	X	X	X	DA11 MSB	DA10	DA9	DA8

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